DHARMSINH DESAI UNIVERSITY

NADIAD 387001.
Website: www.ddu.ac.in

TENDER NOTICE

Quotations are invited for the purchase of **VLSI Design Tool-set - Cadence Standard Bundle** for the laboratories of Department of Electronics & Communication, so as to reach the undersigned on or before **12:30 pm on 29/11/2023.**

(Dr. H. M. Desai)
Vice Chancellor

Major Specifications

Descriptions	User/Task	Quantity
Cadence university Standard Bundle - 3 years term-based licenses	**10**	**1**

Specifications: Standard Bundle Specification

Conformal® Low Power GXL
GenusTM Low Power Option, GenusTM Physical Option, GenusTM Synthesis Solution
Cadence® SKILL Development Environment
Virtuoso® Schematic Editor Verilog Interface
Virtuoso® AMS Designer Environment
Virtuoso® Schematic Editor XL
Virtuoso® ADE Assembler
Virtuoso® Layout Suite GXL
VoltusTM-Fi Custom Power Integrity Solution XL
InnovusTM Mixed Signal Option
InnovusTM Hierarchical Design Option
InnovusTM Implementation System
JasperGold® Formal Verification Platform
Modus DFT Option
Modus ATPG - Distributed Base
InnovusTM DFM Option
Pcell Generator
Cadence® PegasusTM 16nm Node
Cadence® PegasusTM Design Rule Check
Cadence® PegasusTM Layout vs. Schematic Check
Cadence® PegasusTM DFM Fill
Cadence® PegasusTM Results Viewer
Cadence® PegasusTM Programmable Electrical Rule Check
Cadence® PegasusTM Interactive
Cadence® PegasusTM Design Review
Cadence® PegasusTM User Interface
Cadence® PegasusTM Design Review Layout and Mask Data Viewer
Cadence® QuantusTM Extraction XL
Cadence® QuantusTM Advanced Analysis GXL Option
Cadence® QuantusTM Advanced Modeling GXL Option
SigrityTM Advanced SI II
SigrityTM Advanced PI II SystemPI Option
Allegro® Venture PCB Designer
Spectre® RelXpert Reliability Simulator
Spectre® AMS Designer
Spectre® MMSIM with Spectre X Simulator

TempusTM Timing Signoff Solution XL
VoltusTM IC Power Integrity Solution XL (VTS-XL)
TempusTM Timing Signoff Solution ECO
vManagerTM Project Server
vManagerTM Linux Client (Quantity 5)
XceliumTM Single Core
XceliumTM Digital Mixed Signal Option

Terms and Conditions:

• The rates quoted should be inclusive of all taxes.
• The rates quoted must include all necessary packages as mentioned, freight charges, installation and training charges, if any.
• No advance payment will be made. 100% payment against successful installation & working demonstration.
• University will not be bound to accept the lowest quotation and reserves the right to accept or reject any or all quotations without assigning any reason whatsoever.
• Costumers' Certificates indicating satisfactory performance of the similar products and after sales service and the certificate of authorized dealer may add to the merit of the quotation.

F.O.R: Dharmsinh Desai University, Nadiad
Note: The above-mentioned quantities are indicative and may deviate at the time of purchase.

The quotation should be sent to following address in sealed covers, super-scribed at top with "QUOTATION FOR VLSI DESIGN TOOL-SET - CADENCE STANDARD BUNDLE - EC DEPARTMENT" and addressed to,

The Vice Chancellor **21-11-2023**
Dharmsinh Desai University,
P. O. Box No. 35, College Road, Nadiad- 387001